SPICE Modeling for Integrated Circuits

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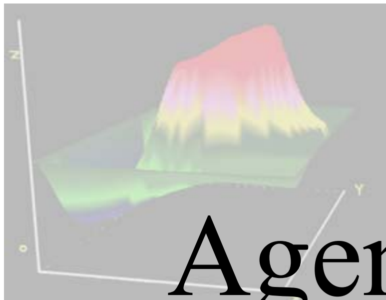
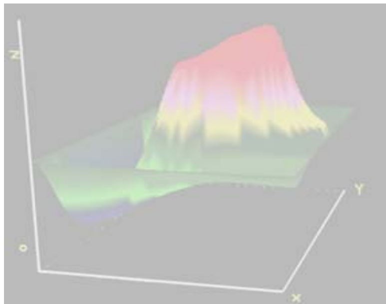


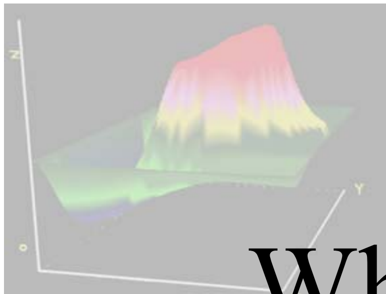
Agenda

- SPICE defined
- Buffer Modeling
- Transistor Model Versions
- Variations to Model
- A Test Case
- Summary



What is SPICE?

- Simulation Program with Integrated Circuit Emphasis
  - A collection of circuit elements with ‘k’ nodes
  - Matrix element solution of circuit.
  - Useful for reasonably accurate modeling of complex integrated circuits.
  - Widely available

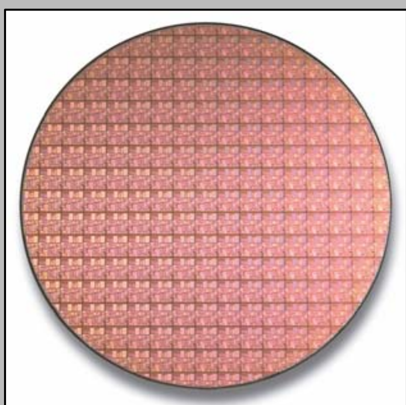


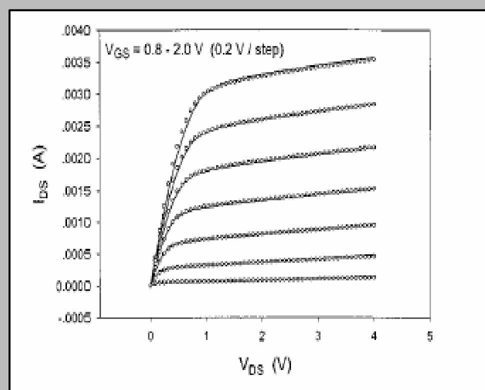
When IBIS? -- When SPICE?

	IBIS	SPICE
Computational Efficiency	Good	From good to poor
Model Complexity	Usually fairly simple	Complex depending upon the needs
Accuracy	From good to poor	Typically good
Applications	Signal Integrity	Signal and power integrity
Programs	Small number	Large number
I/O Circuit Cells	Very large	Limited

Where did SPICE deck come from?

- Device is probed on wafer or package
- Characteristics of device are plotted
- Curve-fitting of device characteristics
- SPICE model generated

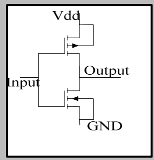





```
.model NMOS NMOS*
****************
+Level=49
+version=3.22
+paramchk=1
+Tnom=27.0
+Nch= 2.498E+17  Tox=9E-09 Xj=1.00000E-07
+Lint=9.36e-8 Wint=1.47e-7
+Vth0= .6322    K1= .756  K2= -3.83e-2  K3= -2.612
+Dvt0= 2.812  Dvt1= 0.462  Dvt2=-9.17e-2
+Nlx= 3.52291E-08  W0= 1.163e-6
+K3b= 2.233
+Vsat= 86301.58  Ua= 6.47e-9  Ub= 4.23e-18  Uc=-4.706281E-11
+Rdsw= 650  U0= 388.3203 wr=1
+A0= .3496967 Ags=.1    B0=0.546    B1= 1
+Dwg = -6.0E-09 Dwb = -3.56E-09 Prwb = -.213
+Keta=-3.605872E-02  A1= 2.778747E-02  A2= .9
•              …
•              …
**************
***End model***
```

What is a Transistor Model in SPICE?

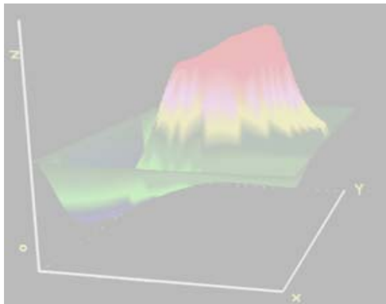
- equivalent parameters in simple deck
- equations from BSIM 3 model.



- *****************
- .model NMOS NMOS*
- *****************
- +Level=49
- +version=3.22
- +paramchk=1
- +Tnom=27.0
- +Nch= 2.498E+17 Tox=9E-09 Xj=1.00000E-07
- **+Lint=9.36e-8 Wint=1.47e-7**
- **+Vth0= .6322 K1= .756 K2= -3.83e-2 K3= -2.612**
- +Dvt0= 2.812 Dvt1= 0.462 Dvt2=-9.17e-2
- …
- +Cdsc=-2.147181E-05
- +Cdscb= 0 Dvt0w = 0 Dvt1w = 0 Dvt2w = 0
- +Cdscd = 0 Prwg = 0
- …
- +Wl = 0 Ww = -1.420242E-09 Wwl = 0
- +Wln = 0 Wwn = .2613948 Ll = 1.300902E-10
- +Lw = 0 Lwl = 0 Lln = .316394
- +Lwn = 0
- +kt1=-.3 kt2=-.051
- ….
- ***************
- ***End model***
- ***************

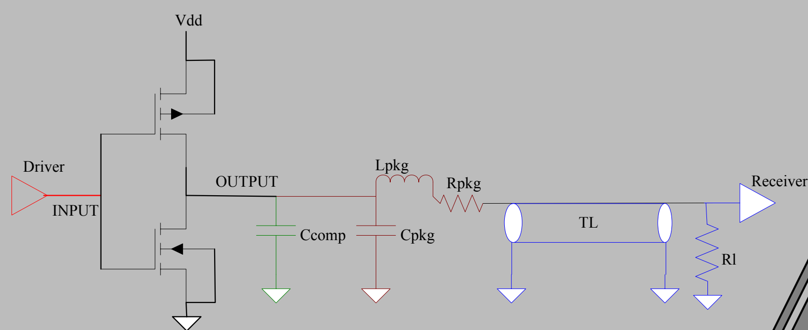
$$r_0 = \left[\frac{\partial I_D}{\partial V_{DS}}\right]^{-1} = \left[\frac{k'}{2}\frac{W}{L}\lambda\left(V_{GS}-V_{TH}\right)^2\right]^{-1} = \frac{V_{DS}+1/\lambda}{I_D}$$

$$i_d = \frac{\partial I_D}{\partial V_{GS}}v_{gs} + \frac{\partial I_D}{\partial V_{BS}}v_{bs} + \frac{\partial I_D}{\partial V_{DS}}v_{ds}$$



Buffer Modeling with SPICE

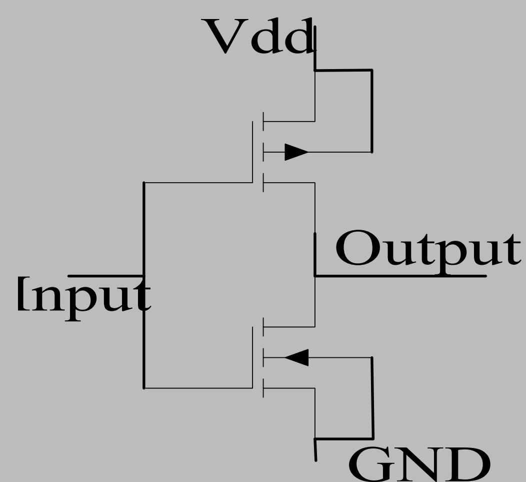
- Drivers & Rationale
  - Wish to emulate the waveshaping of source
  - Determine signal and data integrity of link
  - Design tool…

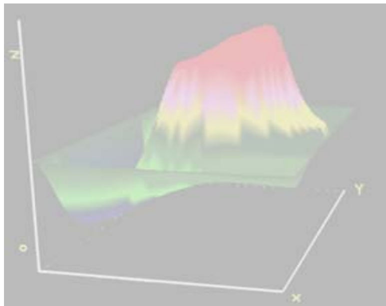


SPICE
Model

Typical SPICE Model for Totempole

```
…
.include component.inc
X_totem Input  Output Vdd GND component
…
```





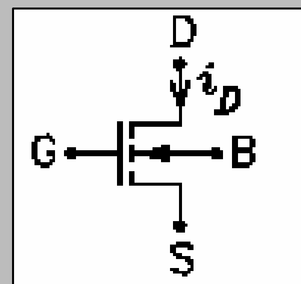
Circuit Level Model

```
*********************
***Component130nm***
*********************
.subckt component130nm NGateP NDrainP NSourceP NSourceN
m_pmos01 NDrainP  NGateP NSourceP NSourceP CMOSP L=0.12u W=20u
m_pmos01 NDrainP  NGateP NSourceP NSourceP CMOSP L=0.12u W=20u
m_pmos01 NDrainP  NGateP NSourceP NSourceP CMOSP L=0.12u W=20u
…
m_nmos01 NDrainP  NGateP NSourceN NSourceN CMOSN L=0.12u W=20u
m_nmos01 NDrainP  NGateP NSourceN NSourceN CMOSN L=0.12u W=20u
m_nmos01 NDrainP  NGateP NSourceN NSourceN CMOSN L=0.12u W=20u
m_nmos01 NDrainP  NGateP NSourceN NSourceN CMOSN L=0.12u W=20u
…
.ends
```

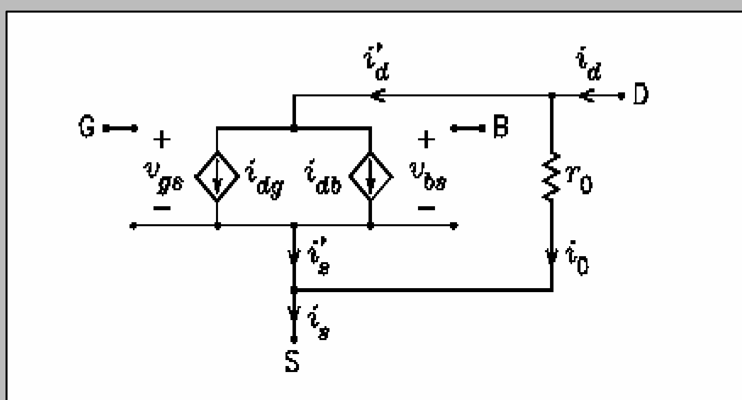
Transistor Model Versions

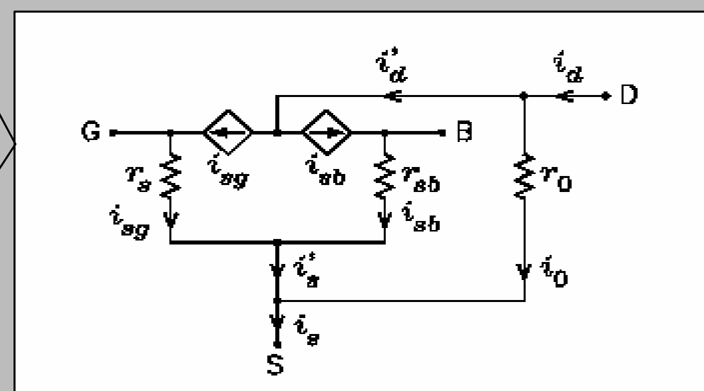
- History
- Transistor Model Versions
  - Level 1-3
  - BSIM1-3
  - HSPICE
- Complexity?

High Level Transistor Circuit Models



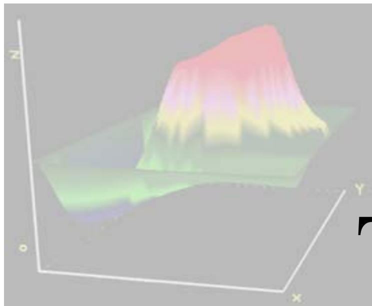
- Enhancement mode MOSFET





- Hybrid-π model
- T- model

- Small Signal Equivalent Models



Transistor level models…

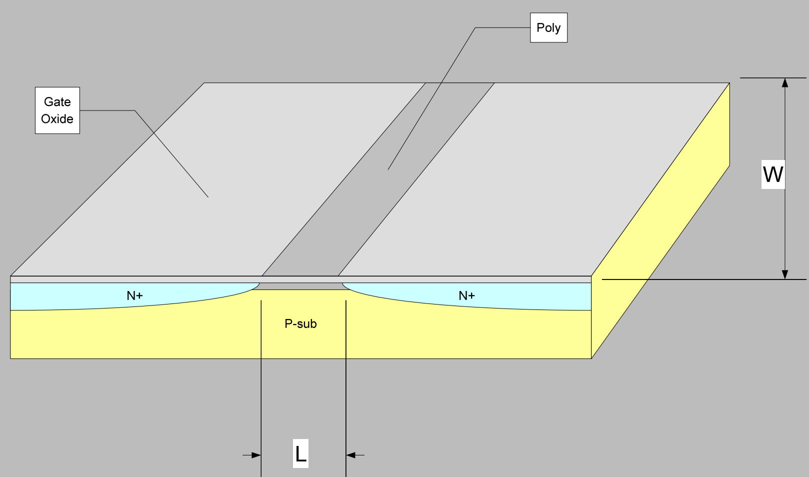
```
.MODEL CMOSN NMOS ( LEVEL   = 49
+VERSION = 3.1          TNOM    = 27           TOX     = 3.2E-9
+XJ      = 1E-7         NCH     = 2.3549E17    VTH0    = 0.0667993
+K1      = 0.3050401    K2      = -6.64669E-3  K3      = 1E-3
+K3B     = 6.3909133    W0      = 1E-7         NLX     = 1E-6 …
```

What does this all mean….??

```
.MODEL CMOSP PMOS ( LEVEL   = 49
+VERSION = 3.1          TNOM    = 27           TOX     = 3.2E-9
+XJ      = 1E-7         NCH     = 4.1589E17    VTH0    = -0.2130346
+K1      = 0.1106589    K2      = 0.0707348    K3      = 0
+K3B     = 14.4425626   W0      = 1E-6         NLX     = 9.045662E-7 …
```

Transistor operation effects (what happens?)

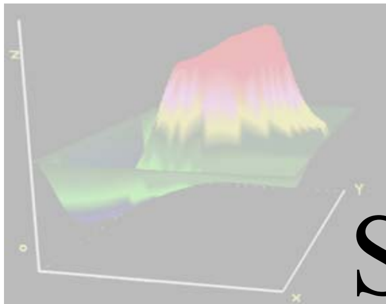
- Transistor model parameter effects
- Variations in geometry and materials prediction



- Key parameters which may vary in process variability may often need to be considered in extraction process for accuracy

Buffer Circuit

- Considerations back to model
  - Layout
  - Interconnections
  - Process
  - Extraction
  - Supplier

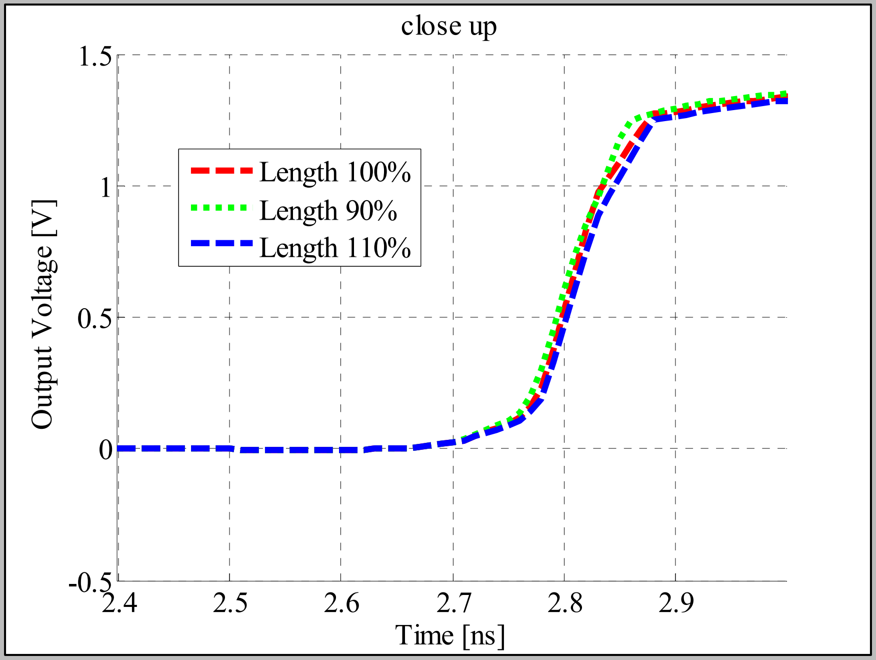


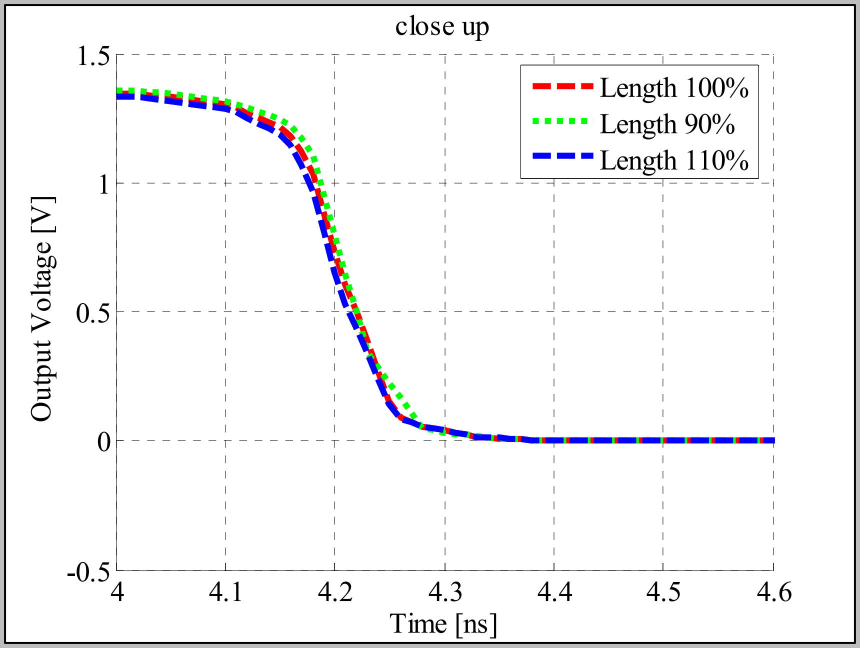
Some Variations in model

- Variations in process need to be accounted for in model generation and parameter extraction.
  - Threshold voltage - V_{TO}
  - Transconductance coefficient K_P
  - Transistor width - W
  - Transistor length - L
- Model ‘binning’
- Added parameters and equations for BSIM
- Packaging anomalies

Results from modeling – first pass with parameters…

- Variations due to process





Summary

- Modeling Strategy
- Validation
- Limitations of Model – BSIM, etc.
- Know the source of model…

References

[1] IBIS Specifications available at http://www.eigroup.org/ibis/specs.htm

[2] Arpad Muranji, "Introduction to IBIS models and IBIS model making", Intel Corporation, Folsom CA, November 3rd-4th 2003.

[3] Stephen Peters (IBIS Open Forum), "IBIS forum I/O buffer modeling cookbook", Revision 2.0X, 1997.

[4] Bob Roos, "IBIS present and future", 7th IEEE Workshop on Signal Propagation on Interconnects, Siena, Italy, May 11th-14th 2003

[5] Mercedes Casamayor, "A first approach to IBIS models: what they are and how are they generated", AN-715Application Note, Analog Device.

[6] "IBIS behavioral models" TN-00-07 Technical Note, Micron.

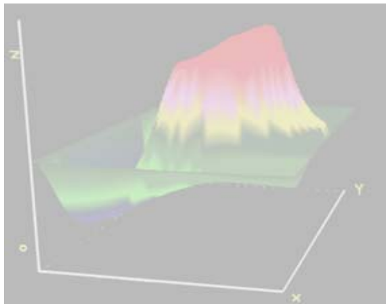
[7] "Validating and using IBIS files", Revision 1.0, National Semiconductor Corporation, Interface Product Group, January 2003.

[8] Vadym Heyfitch, " What makes a better I/O driver model", International Cadence Usergroup.

[9] Microelectronics, Millman-Grabel, McGraw-Hill, 2nd Ed. 1984

[10] MOSFET Modeling with SPICE, Foty, Prentice-Hall, 1997

Backup



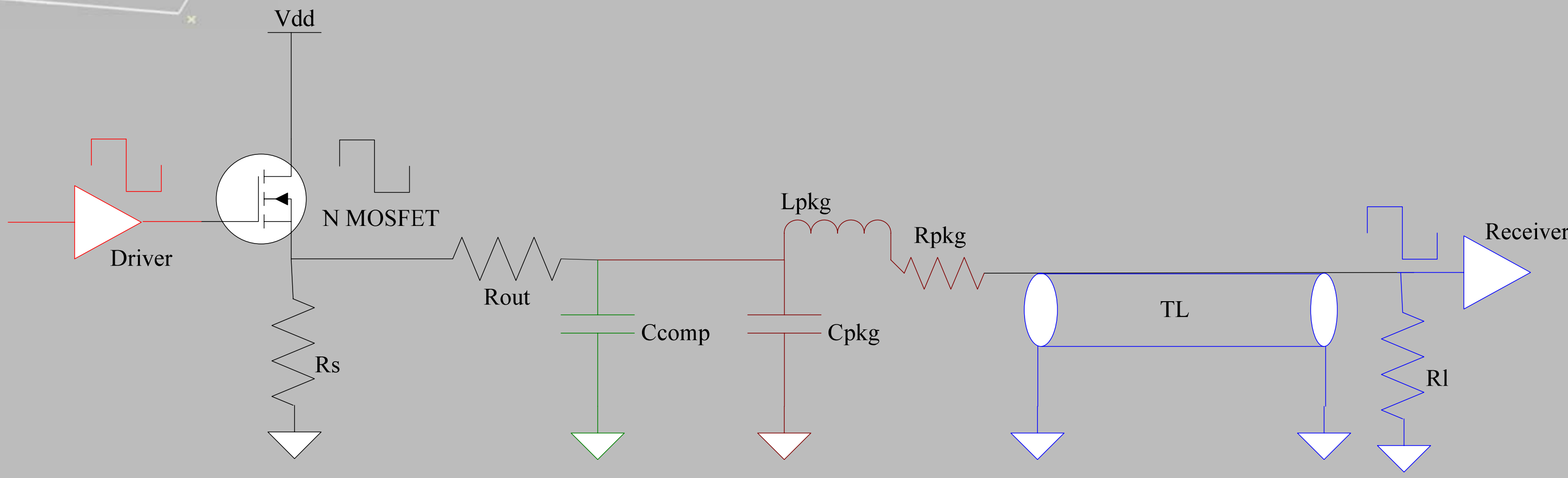
SPICE Model

- The SPICE model:
  – Mere translation of each circuit component, i.e., MOSFET driver, resistors, transmission tine, etc., into a line of code representing the element itself between two or more voltage nodes.

- For this example:
  – Generic Driver has no output impedance, while the generic Receiver has infinite input impedance.

- The choice of the MOSFET parameters, such as V_{TO}, K_P, *l* and *w*, is intended to achieve low output impedance – *but still be practical!*

Simple I/O Circuit Example



- Let’s consider a non-inverting MOSFET circuit configuration with the output connected to a 50 Ω TL through a 50 Ω load and some parasitic elements.
- The MOSFET is excited by a generic Driver, whose voltage swings between 3.3V and GND, whereas a generic Receiver in // with a 50 Ω load terminates the 50 Ω TL.
- The MOSFET works as a source follower with the Drain connected to a DC voltage source of 3.3 V and the Source connected to the ground through a 150 Ω load.
- The circuit is studied only for testing purposes, not for practical circuit design.